This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A semiconductor device provided with a memory cell including a first driver transistor, a second driver transistor, a first transfer transistor, a second transfer transistor, a first load transistor and a second load transistor, the semiconductor device comprising:

figs. 1-13

a first gate-gate electrode layer including a gate electrode of the first load transistor and a gate electrode of the first driver transistor;

a second gate-gate electrode layer including a gate electrode of the second load transistor and a gate electrode of the second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer;

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer; and

a first active region in which the first load transistor is provided,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and

wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region.

2. (Original) The semiconductor device according to claim 1, wherein the first protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors are provided.

3. (Original) The semiconductor device according to claim 1, wherein a part of the first active region and the first protruded active region form an L-shape.

4. (Original) The semiconductor device according to claim 1, comprises:

a second active region in which the second load transistor is provided; and

a second protruded active region provided in a manner to protrude from an end portion of the second active region.

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5. (Original) The semiconductor device according to claim 4, wherein the second protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors are provided.

6. (Original) The semiconductor device according to claim 4, wherein a part of the second active region and the second protruded active region form an L-shape.

7. (Original) The semiconductor device according to claim 1,

wherein the first drain-gate wiring layer is electrically connected to the second drain-drain wiring layer through a contact section, and

wherein the second drain-gate wiring layer is electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

8. (Original) The semiconductor device according to claim 1, wherein the first drain-gate wiring layer is located in a layer lower than the second drain-gate wiring layer.

9. (Original) The semiconductor device according to claim 1, wherein the first drain-gate wiring layer is located in a layer in which the first gate-gate electrode layer is provided.

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10. (Original) The semiconductor device according to claim 1, wherein the second drain-gate wiring layer is formed across a plurality of layers.

11. (Original) The semiconductor device according to claim 10,

wherein the second drain-gate wiring layer includes a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and

wherein the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer.

12. (Original) The semiconductor device according to claim 11, wherein the upper layer is electrically connected to the lower layer through a contact section.

13. (Original) The semiconductor device according to claim 11,

wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in a first conductive layer,

wherein the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer, and

wherein the upper layer is located in a third conductive layer.

14. (Currently Amended) The semiconductor device according to claim [1] 13, wherein the second conductive layer is a nitride layer of a refractory metal.

15. (Original) The semiconductor device according to claim 1, wherein the second conductive layer has a thickness of 100 nm to 200 nm.

Cont Q2 fig. 2

16. (Original) A semiconductor device using as a memory cell a flip-flop including a first load transistor, a first driver transistor, a second load transistor and a second driver transistor,

wherein the first and second load transistors in one memory cell are disposed symmetrically about a straight line extending in a gate width direction between drain regions of the first and second load transistors, and

wherein each of the drain regions of the first and second load transistors includes a protruded active region protruding in the gate width direction beyond an end of a channel region.

17. (Original) A memory system provided with the semiconductor device defined in any one of claims 1 to 16.

18. (Original) An electronic apparatus provided with the semiconductor device defined in any one of claims 1 to 16.